anticipated by Barker, and claim 32 is not rendered obvious over Barker, for at least the following reasons.

Claim 15 recites the following:

> a plurality of computing cells arranged in a multidimensional matrix, the plurality of computing cells capable of simultaneously manipulating a plurality of data, each of the plurality of ***computing cells including***:
>
> an input interface for receiving a plurality of input signals,
>
> a plurality of logic members, at least one of the plurality of logic members coupled to the input interface,
>
> at least one coupling unit selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals to arithmetic-logically configure the computing cell prior to processing the input signals, wherein coupled logic members perform select arithmetic-logic operations on the input signals to process the input signals, the select arithmetic-logic operations being dependent on the at least one of the plurality of configuration signals,
>
> a register unit selectively storing a portion of the processed input signals, and
>
> an output interface for transmitting the processed input signals,
>
> wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells; and
>
> a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells. . . .

It is unclear from the Office Action upon which element or elements described in Barker the Examiner relies with respect to "computing cells." The Examiner, for example, cites to a number of figures and columns of Barker, but does not identify any particular elements. The Examiner is respectfully requested to identify the particular elements upon which the Examiner relies for each of Applicants' claim elements.

If the Examiner relies on the PME described in Barker as a "computing cell," it is respectfully submitted that a PME does not include logic elements which are selectively coupled via a coupling unit to arithmetic-logically configure the PME, wherein coupled logic members perform select arithmetic-logic operations on input signals to process the input signals. In Barker, each PME is a self-contained stored program microcomputer. Col. 27, lines 23-26. The multiplexers in a PME, for example, appear to be used merely to select inputs to an ALU and PME registers. Col. 29, lines 51-56. These multiplexers are not used to selectively couple logic elements to arithmetic-logically configure or reconfigure the PME.

Claims 16-31, 33 and 34 all depend, directly or indirectly from claim 15. Accordingly, the argument presented above in connection with claim 15 applies equally to claims 16-34.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate any of claims 15-31, 33 and 34.

Claim 32 depends from claim 15. Accordingly, the arguments presented above in connection with claim 15 and Barker apply equally to claim 32. Moreover, claim 32 further recites the following:

> . . . wherein that at least another of the plurality of lines are divided in a plurality of segments, wherein each of the plurality of segments is connected to at least another one of the plurality of segments by a tristate-bus-driver.

With respect to this feature, the Examiner relies on subject matter to which the Examiner has taken Official Notice. Respectfully, it is submitted that the use of a tristate-bus-driver in combination with other features of the claimed invention, is neither taught nor suggested by the prior art. In accordance with MPEP 2144.03, the Examiner is requested to either provide an affidavit if the rejection is based on facts within th personal knowledge of the Examiner, or provide a

Applicants with a prior art reference supporting the Examiner's rejection. Applicants respectfully submit that it would not be obvious to a person of ordinary skill in the art to provide a tristate-bus-drive for connecting segments of lines in a reconfigurable processor.

In view of the foregoing, withdrawal of the rejections of claims 15-34 is, therefore, requested.

Claims 35-46

Claims 35-46 stand rejected under 35 U.S.C. § 102(e) over Barker. It is respectfully submitted that none of claims 35-46 is anticipated by Barker, for at least the following reasons.

Claim 35 recites the following:

> . . . a plurality of computing cells arranged in a multidimensional matrix, each of the plurality of computing cells being arithmetic-logically configurable and reconfigurable, each of the plurality of computing cells capable of processing a first plurality of data words simultaneously with the processing of a second plurality of data words by others of the plurality of computing cells, wherein each of the plurality of computing cells is arithmetic-logically configured by a first configuration signal to perform a first select arithmetic-logic operation, and wherein each of the plurality of computing cells is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second select operation . . . .

Claims 36-46 depend from claim 35.

As discussed above in connection with claim 15, Barker does not teach or suggest an arithmetic-logically configurable and reconfigurable computing cell. In Barker,

each PME has a "circuit switched mode" of I/O in which one of its four input ports can be switched directly to ones of its four output ports. Col. 27, lines 51-53. However, this capability does not involve arithmetic-logic reconfiguration. According to Barker, selection of the source and destination of the "circuit switch" is under control of the software executing on the PME; thus, it does not appear to involve arithmetic-logic reconfiguration. Each PME can also operate in SIMD or in MIMD mode. However, this does not appear to involve any arithmetic-logic reconfiguration.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate any of claims 35-46. Withdrawal of the rejection of claims 35-46 under 35 U.S.C. § 102(e) is, therefore, requested.

Claims 47-56

Claims 47-56 stand rejected under 35 U.S.C. § 102(e) over Barker. It is respectfully submitted that Barker does not anticipate any of claims 47-56, for at least the following reasons.

Claim 47 recites the following:

> a programmable logic device, the programmable logic device including a plurality of logic elements arranged in a multidimensional matrix, each of the plurality of logic elements being arithmetic-logically configurable and reconfigurable, each of the plurality of logic elements capable of processing a first plurality of binary signals simultaneously with the processing of a second plurality of binary signals by others of the plurality of logic units, wherein each of the plurality of logic elements is arithmetic-logically configured to perform a first select arithmetic-logic operation by a first configuration signal, and wherein each of the plurality of logic elements is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second configuration signal different than the first configuration signal, the first select operation being different than the second

select operation,

Claims 48-56 depend from claim 47.

Barker does not describe or even arithmetic-logic configuration and reconfiguration of logic elements. As discussed above in connection with claims 15 and 35, the PMEs of Barker are capable of operating in different modes. However, nothing within Barker suggests that this involves any sort of arithmetic-logical reconfiguration, under control of configuration signals or otherwise.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate any of claims 47-56. Withdrawal of the rejection of claims 47-56 under 35 U.S.C. § 102(e) over Barker is, therefore, requested.

Claims 57-61

Claims 57-61 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that none of claims 57-61 is anticipated by Barker, for at least the following reasons.

Claim 57 recites the following:

> a first compiler for individually accessing and individually configuring at least some of the cells, the first compiler selectively grouping the at least some of the cells with neighboring cells into functional units to perform a first function, the first compiler further selectively regrouping selected ones of the at least some of the cells into different functional units to perform a second function different than the first function while simultaneously others of the at least some of the cells process data.

Claims 58-61 depend from claim 57. It is unclear upon which features of Barker the Examiner relies on with respect to the above-cited feature of claim 57. In particular, with respect to claim 57, the Examiner merely indicates that this claim is "rejected for the same reasons as cited in the rejections of claims 15-47," none of which claims recite grouping and

regrouping cells. The Examiner is requested to clarify the rejection, and identify with some specificity the elements upon which the Examiner relies. However, nothing within Barker appears to suggest selectively grouping and regrouping PMEs to perform functions, while other PMEs process data or otherwise.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate any of claims 57-61. Withdrawal of the rejection of claims 57-61 under 35 U.S.C. § 102(e) is, therefore, requested.

Claims 62-68

Claims 62-68 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that Barker does not anticipate any of claims 62-68, for at least the following reasons.

Claim 62 recites the following:

> cells arranged in a multi-dimensional pattern, at least one of the cells being selectively coupled to a first one of the cells to form a first functional unit at a first time, the first functional unit performing a first function, the at least one of the cells capable of being regrouped with a second one of the cells to form a second functional unit at a second time different from the first time, the second functional unit performing a second function different from the first function, the at least one of the cells regrouping as a function of reconfiguration data; and
>
> a first compiler receiving state information regarding the state of the first functional unit and transmitting reconfiguration data to the at least one of the cells as a function of the received state information.

Claims 63-68 depend from claim 62.

The Examiner did not address the subject matter of claim 62, accordingly, it is unclear upon which elements of Barker the Examiner relies in the connection with the rejection of claims 62-68. It appears, for example, that in Barker, each PME can control communication with neighboring PMEs. It does

not appear that state information regarding any functional units is received by any unit, or that reconfiguration data is transmitted as a function thereof.

In view of the foregoing, it is respectfully submitted that none of claims 62-68 is anticipated by Barker. Withdrawal of the rejection of claims 62-68 under 35 U.S.C. § 102(e) is, therefore, requested.

Claims 69-71

Claims 69-71 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that none of claims 69-71 is anticipated by Barker, for at least the following reasons.

Claim 69 recites the following:

> grouping at least some of the cells into functional units;
> processing data by the functional units; and
> receiving, by a reconfiguration unit, state information regarding at least one of the functional units.

Claims 70 and 71 depend from claim 69.

The Examiner did not specifically address the subject matter of any of claims 69-71; thus, the basis for the rejection is unclear. Although Barker mentions that the system can select groups of PMEs for a function (col. 16, lines 23-24), it does not appear that state information is transmitted regarding functional units.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate any of claims 69-71. Withdrawal of the rejection of claims 69-71 under 35 U.S.C. § 102(e) over Barker is, therefore, requested.

Claims 72 and 73

Claims 72 and 73 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that Barker does not anticipate either of claims 72 or 73, for at le st the following reasons.

Claim 72 recites the following:

> individually configuring at least some of the cells to form functional units;
> processing data by at least some of the functional units; and
> receiving, by a reconfiguration unit, state information regarding at least one of the functional units; and
> individually reconfiguring at least one cell of at least one of the functional units to form a different functional unit as a function of the state information, while simultaneously others of the functional units continue processing data

Claim 73 depends from claim 72.

With respect to claims 72 and 73, the Examiner did not specifically identify upon which features of Barker the Examiner relies as the basis of rejection. Barker describes, for example, that the system can select groups of PMEs for a function. There does not appear to be any indication that a reconfiguration unit receives state information regarding a group of PMEs, much less, that PME are reconfigured as a function of such state information.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate either of claims 72 and 73. Withdrawal of the rejection of claims 72 and 73 under 35 U.S.C. § 102(e) is, therefore, requested.

Claims 74-76

Claims 74-76 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that Barker does not anticipate any of claims 74-76, for at least the following reasons.

Claim 74 recites the following:

> grouping at least some of the cells into functional units;
> enabling by a state machine the at least some of the cells;
> after the enabling step, processing data by the functional units;
> receiving, by a reconfiguration unit, state information regarding at least one of the functional units;

transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information;

disabling by the state machine at least some of the cells of the at least one of the function units while others of the function units are still enabled; and

after the disabling step, reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data.

Claims 75 and 76 depend from claim 74. The Examiner did not provide specific reasons for rejecting any of claims 74-76, thus, the basis for the rejection is unclear.

As discussed above, Barker mentions that PMEs can selects groups of PMEs for a function. However, Barker does not appear to teach or suggest receiving by a reconfiguration unit, state information regarding a functional unit, much less, transmitting configuration data in response thereto.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate any of claims 74-76. Withdrawal of the rejection of claims 74-76 under 35 U.S.C. § 102(e) is, therefore, requested.

Claim 77

Claim 77 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that claim 77 is not anticipated by Barker, for at least the following reasons.

Claim 77 recites the following:

enabling by a state machine a transfer of data between a first plurality of the cells depending on the presence of the data and a state of at least some of the cells, the first plurality of the cells being in a READY state for at least one of i) accepting new data, and ii) transmitting a result; and

disabling by a state machine the transfer of the data depending on the presence of the data and the state of at least some of the

cells, the at least some of the cells being in a NOT ready state for accepting the new data and for transmitting the results.

With respect to claim 77, the Examiner has not indicated the particular elements or features of Barker upon which the Examiner relies in connection with the rejection. It is respectfully submitted that Barker does not describe PMEs, much less cells, in a READY state and a NOT ready state. Moreover, there does not appear to be a state machine that enables and disables the transfer of data. As indicated above, it appears that each PME controls communication between itself and neighboring PMEs using bits in a register and software in the PME.

In view of the foregoing, it is respectfully submitted that Barker does not anticipate claim 77. Withdrawal of the rejection of claim 77 under 35 U.S.C. § 102(e) over Barker is, therefore, requested.

Claim 78

Claim 78 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Barker. It is respectfully submitted that Barker does not anticipate claim 78, for at least the following reasons.

Claim 78 recites the following:

> grouping at least some of the cells into functional units;
> enabling by a state machine the at least some of the cells;
> after the enabling step, processing data by the functional units;
> receiving, by a reconfiguration unit, state information regarding at least one of the functional units;
> disabling by the state machine at least some of the cells of the at least one of the function units while others of the function units are still enabled;
> transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information; and

after the disabling step, reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data.

The Examiner did not provide any details as to which elements or features of Barker the Examiner relies in connection with the rejection of claim 77. As discussed above, Applicants submit that Barker does not teach or suggest receiving by a reconfiguration unit state information regarding functional units, let alone, transmitting configuration data as a function thereof.

In view of at least the foregoing, it is respectfully submitted that claim 77 is not anticipated by Barker. Withdrawal of the rejection of claim 77 is, therefore, requested.

Claims 79-83

Claims 79-83 recite further features of the present invention. Support for the subject matter of these claims can be found throughout the Specification.

IDS

On January 12, 2001, Applicants submitted an IDS and a lengthy FORM-1449. However, Applicants have received a copy of only the first page of the initialed FORM-1449. The Examiner is requested to forward to Applicants a complete copy of the initialed FORM-1449 with the next communication.

CONCLUSION

In view of all of the above, it is believed that the rejections of the claims have been obviated, and that claims 15 to 81 are allowable. It is therefore respectfully request d that the rejections be withdrawn, and that the present application issue as early as possible.

Respectfully submitted,

Dated: 2 Nov 2001

By: _____

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CUSTOMER NO. 26646

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as set forth below.

15. (Amended) A massively parallel data processing apparatus comprising:

a plurality of computing cells arranged in a multidimensional matrix, the plurality of computing cells capable of simultaneously manipulating a plurality of data, each of the plurality of computing cells including:

an input interface for receiving a plurality of input signals[;],

a plurality of logic members, at least one of the plurality of logic members coupled to the input interface, [the plurality of logic members processing the plurality of input signals;]

at least one coupling unit selectively coupling at least one of the plurality of logic members to another of the plurality of logic members a function of at least one of a plurality of configuration signals[;] to arithmetic-logically configure the computing cell prior to processing the input signals, wherein coupled logic members perform at least one select arithmetic-logic operation on the input signals to process the input signals, the at least one select arithmetic-logic operation being dependent on the at least one of the plurality of configuration signals,

a register unit selectively storing a portion of the processed input signals[;], and

an output interface for transmitting the processed input signals[;],

wherein the input interface of at least one of the plurality of computing cells is selectively

coupled to the output interface of at least another of the plurality of computing cells; and

a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells.

35. (Amended) A massively parallel data processing apparatus, comprising:

a plurality of computing cells arranged in a multidimensional matrix, each of the plurality of computing cells being arithmetic-logically configurable and reconfigurable, each of the plurality of computing cells capable of processing a first plurality of data words simultaneously with the processing of a second plurality of data words by others of the plurality of computing cells, wherein each of the plurality of computing cells is arithmetic-logically configured by a first [set of] configuration [words] signal to perform a first select arithmetic-logic operation, and wherein each of the plurality of computing cells is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second [set of] configuration [words] signal different than the first configuration signal, the first select operation being different than the second select operation; and

a plurality of buses, wherein each of the plurality of computing cells are connectable to at least one of the plurality of computing cells using at least one of the plurality of buses.

43. (Amended) The massively parallel data processing apparatus of claim 42, further comprising:

a memory, coupled to the compiler, for storing the first [set of] configuration [words] signal and the second [set of] configuration [words] signal.

47. (Amended) A massively parallel data processing apparatus, comprising:

a programmable logic device, the programmable logic device including a plurality of logic elements arranged in a multidimensional matrix, each of the plurality of logic elements being arithmetic-logically configurable and reconfigurable, each of the plurality of logic elements capable of processing a first plurality of binary signals simultaneously with the processing of a second plurality of binary signals by others of the plurality of logic units, wherein each of the plurality of logic elements is arithmetic-logically configured to perform a first select arithmetic-logic operation by a first [set of] configuration [words] signal, and wherein each of the plurality of logic elements is arithmetic-logically reconfigured to perform a second select arithmetic-logic operation by a second [set of] configuration [words] signal different than the first configuration signal, the first select operation being different than the second select operation, the programmable logic device further comprising a plurality of buses, wherein each of the plurality of logic elements are connectable to at least one of the plurality of logic elements using at least one of the plurality of buses; and

at least one memory device coupled to the programmable logic device for storing at least one of i) multiple data to be processed by the programmable logic device, and ii) processing results of the programmable logic device [; and

at least one of i) an interface coupled to at least one external computer and ii) a further memory device coupled to the at least one external computer, for transferring at least one of multiple data to be processed by the programmable logic device and processing results of the programmable logic device].

53. (Amended) The massively parallel data processing apparatus of claim 52, further comprising:

a memory, coupled to the compiler, for storing the first [set of] configuration [words] signal and the second [set of] configuration [words] signal.

69. (Amended) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

grouping at least some of the cells into functional units;

processing data by the functional units; and

receiving, by a reconfiguration unit, state information regarding at least one of the functional units[;

transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information; and

reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data].

72. (Amended) A method for configuring a data processor, the data processor including cells arranged in a multi-dimensional pattern, comprising the steps of:

individually configuring at least some of the cells to form functional units;

processing data by at least some of the functional units; and

receiving, by a reconfiguration unit, state information regarding at least one of the functional units; and

individually reconfiguring at least one cell of at least one of the functional units to form a different functional unit at a function of the state information, while simultaneously others of the functional units continue processing data.

73. (Amended) The method according to claim 72, further comprising the steps of:

[receiving, by a reconfiguration unit, state information regarding at least one of the functional units;]

transmitting, by the reconfiguration unit, reconfiguration data to the at least one cell, wherein the step of reconfiguring includes the step of reconfiguring, by the at least one cell, as a function of the reconfiguration data transmitted by the reconfiguration unit.

Please add the following new claims:

79. (New) The massively parallel data processing apparatus of claim 15, wherein the cell configuration memory is dedicated to storing configuration information.

80. (New) The massively parallel data processing apparatus of claim 47, further comprising:

at least one of i) an interface coupled to at least one external computer and ii) a further memory device coupled to the at least one external computer, for transferring at least one of multiple data to be processed by the programmable logic device and processing results of the programmable logic device.

81. (New) The method of configuring a data processor of claim 69, further comprising:

transmitting, by the reconfiguration unit, respective configuration data to the at least one of the functional units as a function of the received state information; and

reconfiguring at least one of the cells in the at least one of the functional units as a function of the respective configuration data while simultaneously other functional units continue processing data.

82. (New) The massively parallel data processing apparatus according to claim 15, wherein each of the computing cells includes a cell configuration memory adapted to store the at least one of the plurality of configuration signals.

83. (New) The massively parallel data processing apparatus according to claim 17, wherein the selectively coupled computing cells together form a dataflow processor.

84. (New) The massively parallel data processing apparatus according to claim 35, wherein each of the computing cells includes a cell configuration memory adapted to store the first configuration signal and the second configuration signal.

85. (New) The massively parallel data processing apparatus according to claim 35, wherein each of the computing cells includes a plurality of logic members selectively coupled together in accordance with the first set of configuration words to arithmetic-logically configure the computing cell and in accordance with the second set of configuration words to arithmetic-logically reconfigure the computing cell.

86. (New) A massively parallel data processing apparatus comprising:

a plurality of computing cells arranged in a multidimensional matrix, the plurality of computing cells capable of simultaneously manipulating a plurality of data, each of the plurality of computing cells including:

an input interface for receiving a plurality of input signals,

a plurality of logic members, at least one of the plurality of logic members coupled to the input interface,

at least one coupling unit selectively coupling at least one of the plurality of logic members to

another of the plurality of logic members a function of at least one of a plurality of configuration signals,

a cell configuration memory adapted to store the at least one of the plurality of configuration signals,

a register unit selectively storing a portion of the processed input signals, and

an output interface for transmitting the processed input signals,

wherein the input interface of at least one of the plurality of computing cells is selectively coupled to the output interface of at least another of the plurality of computing cells; and

a configuration interface for transmitting the plurality of configuration signals to at least some of the plurality of computing cells to arithmetic-logically configure and arithmetic-logically reconfigure the at least some of the plurality of computing cells.

83. (New) The massively parallel data processing device according to claim 17, wherein the selectively coupled computing cells together form a dataflow processor.